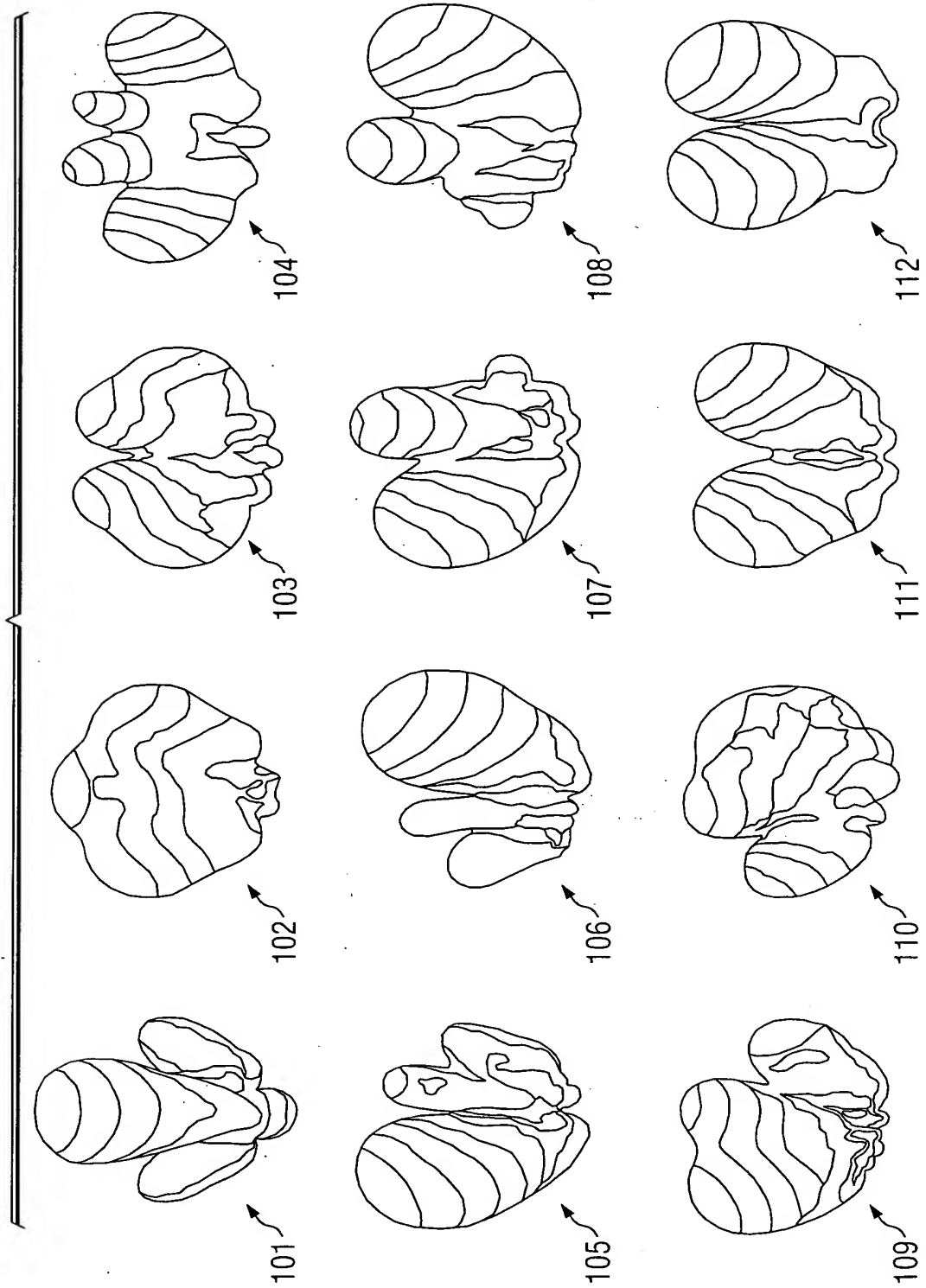
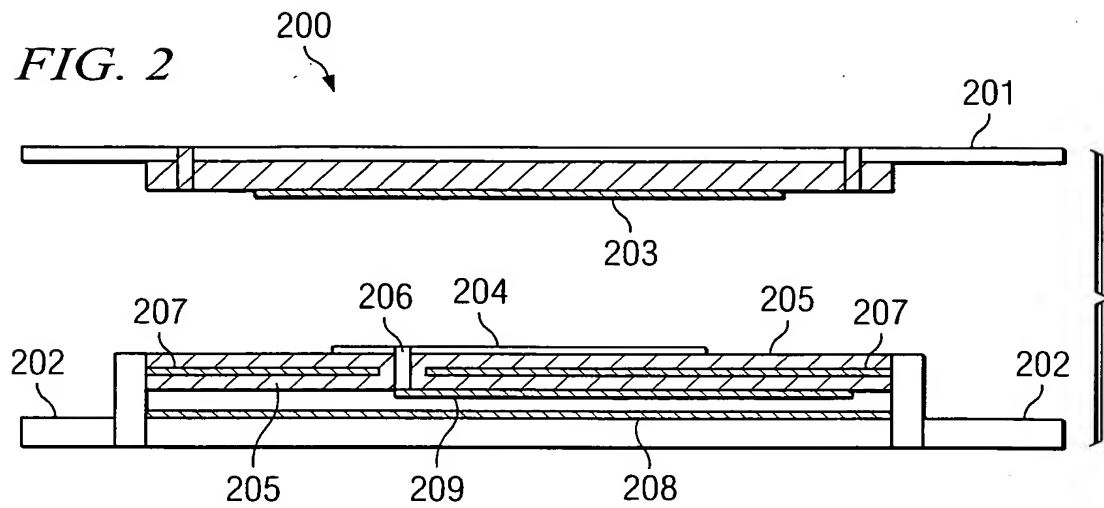
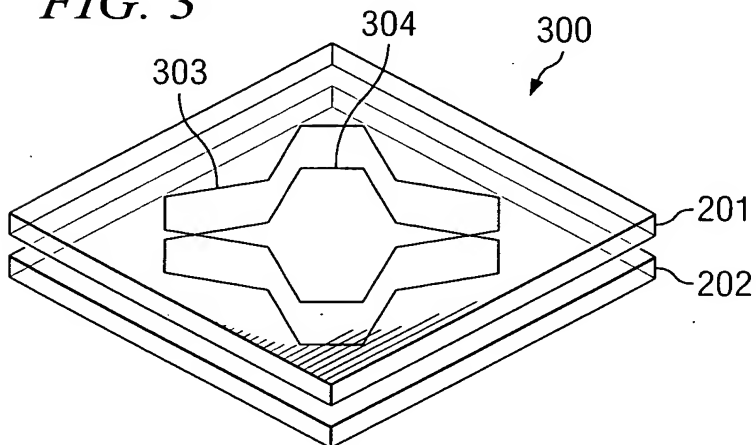
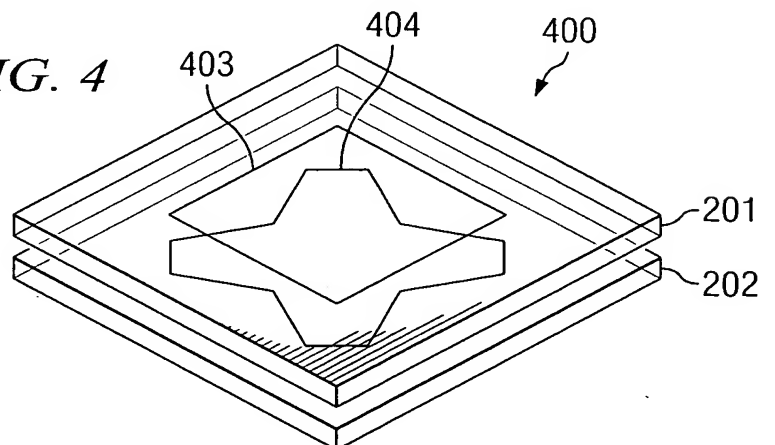


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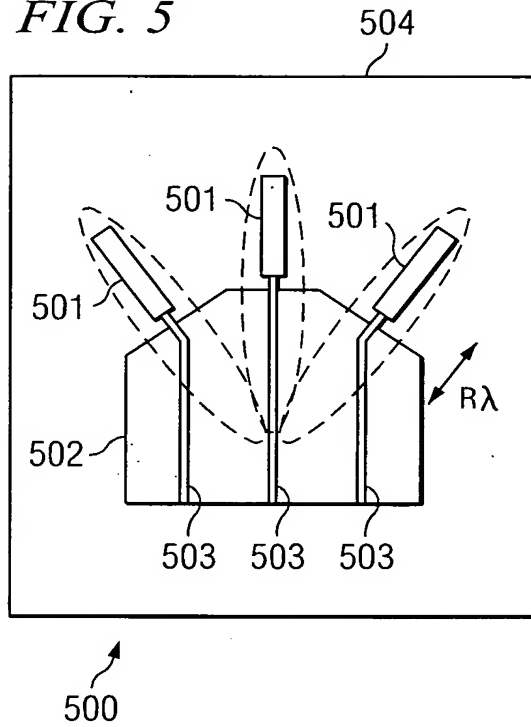
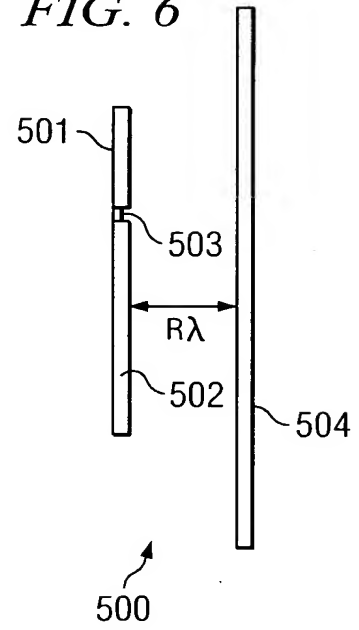
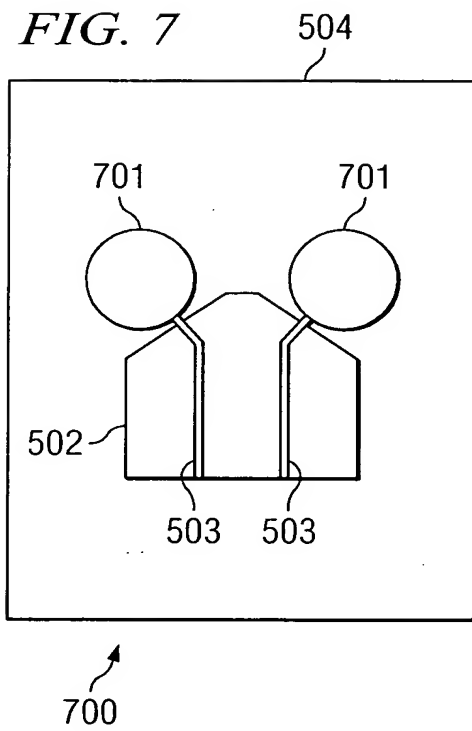
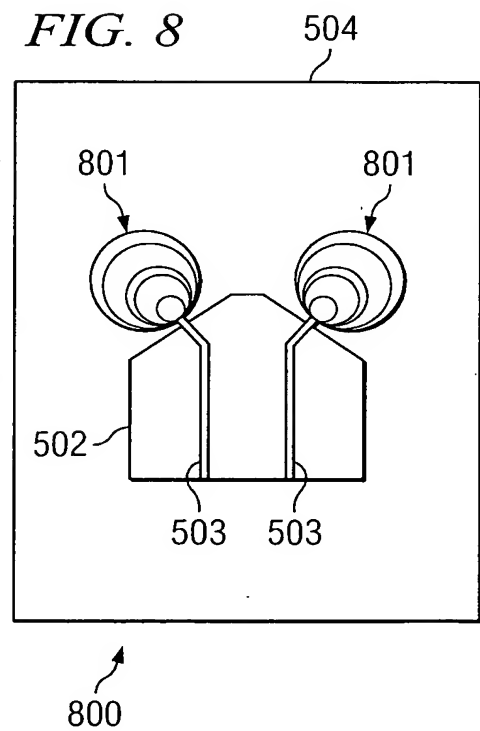
FIG. 1



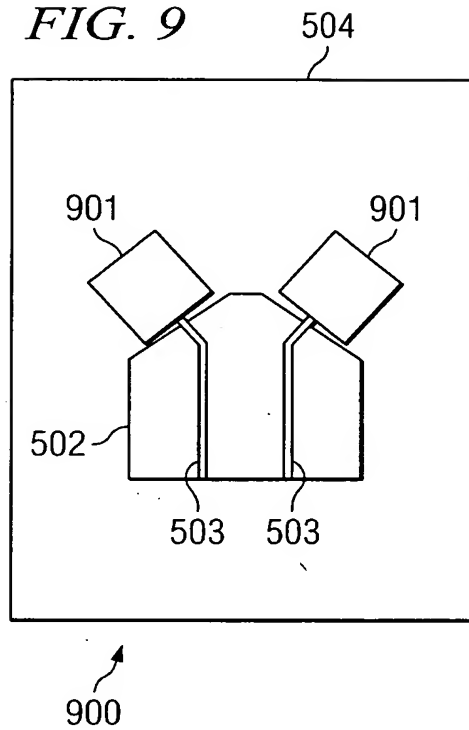
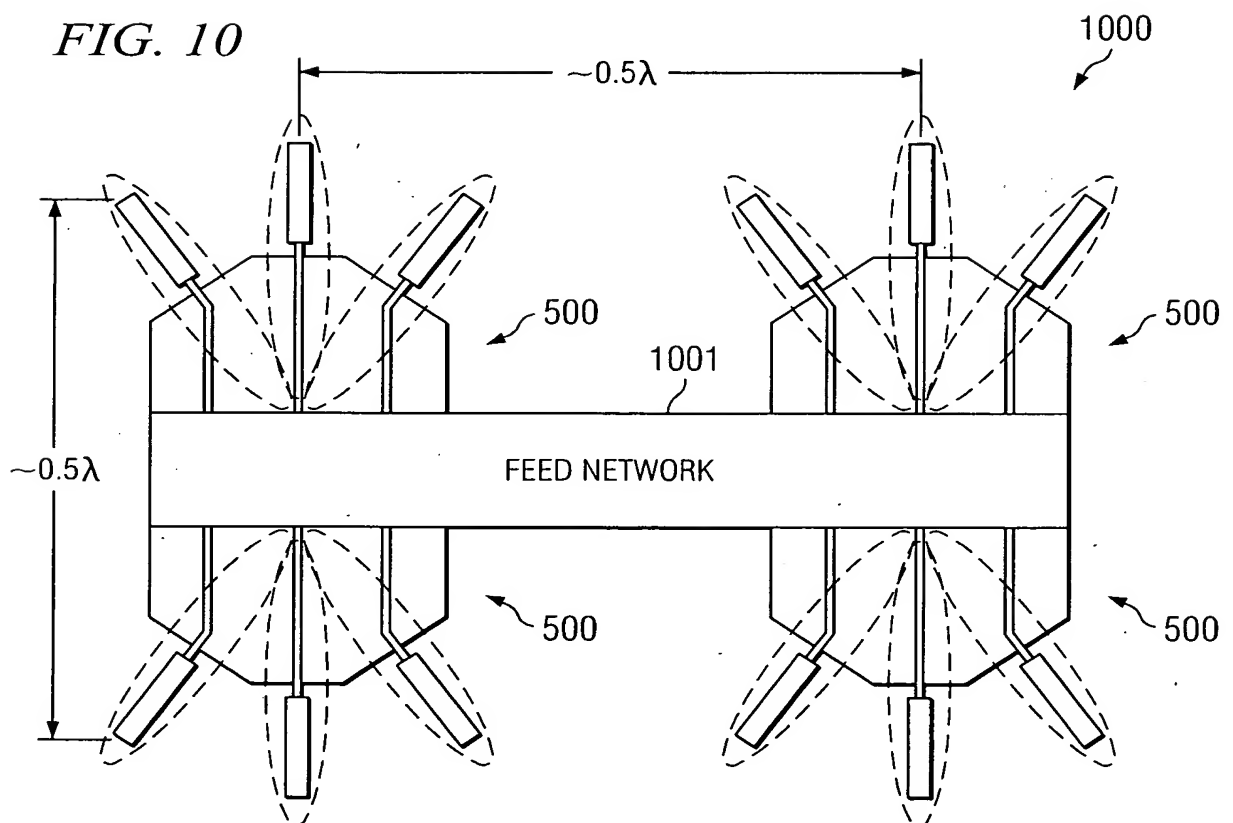
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FIG. 2*FIG. 3**FIG. 4*

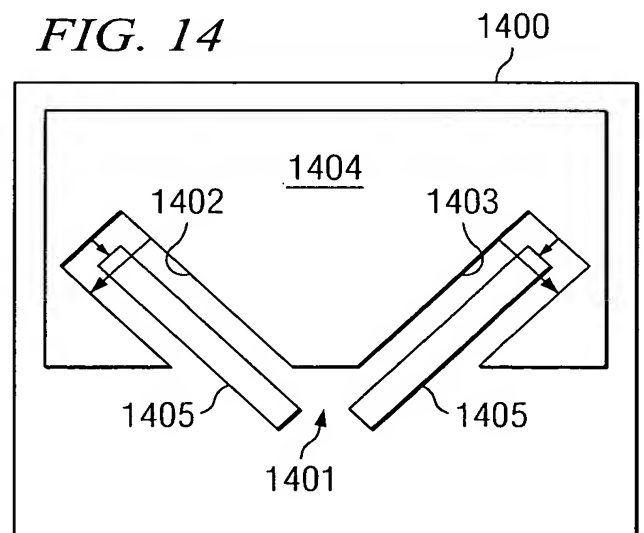
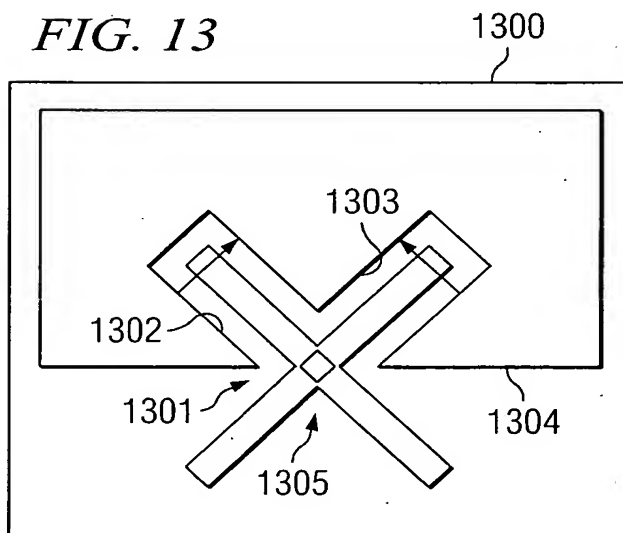
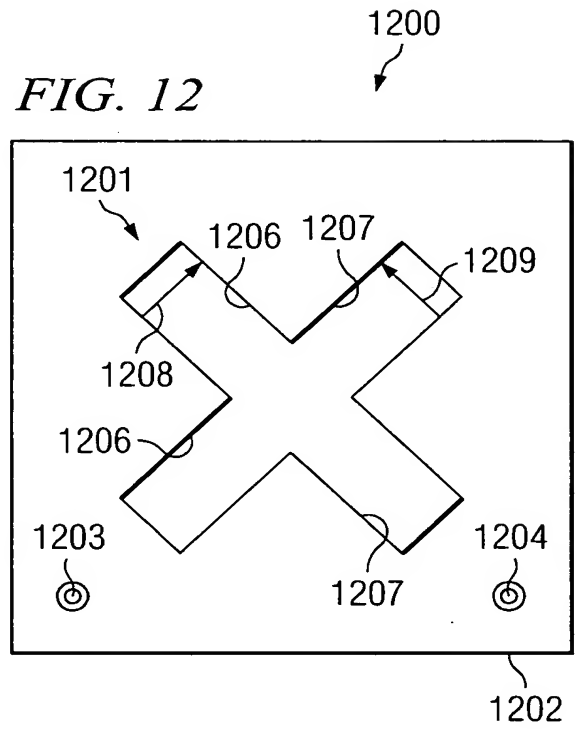
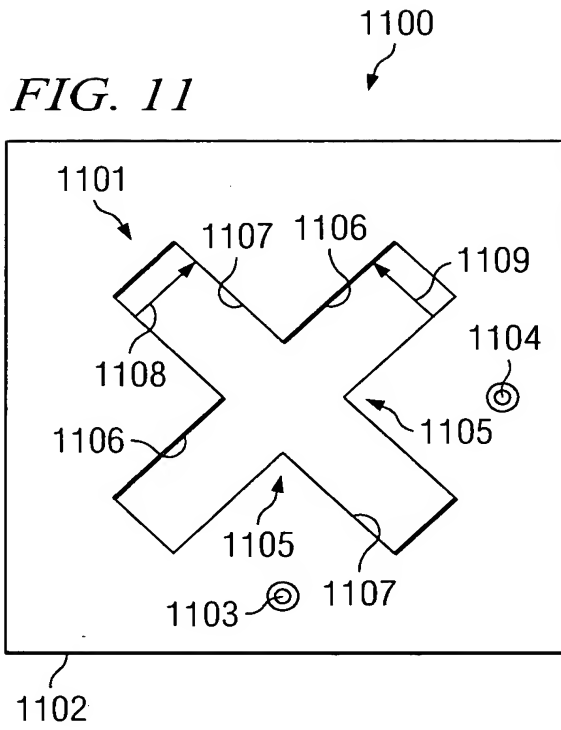
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FIG. 5*FIG. 6**FIG. 7**FIG. 8*

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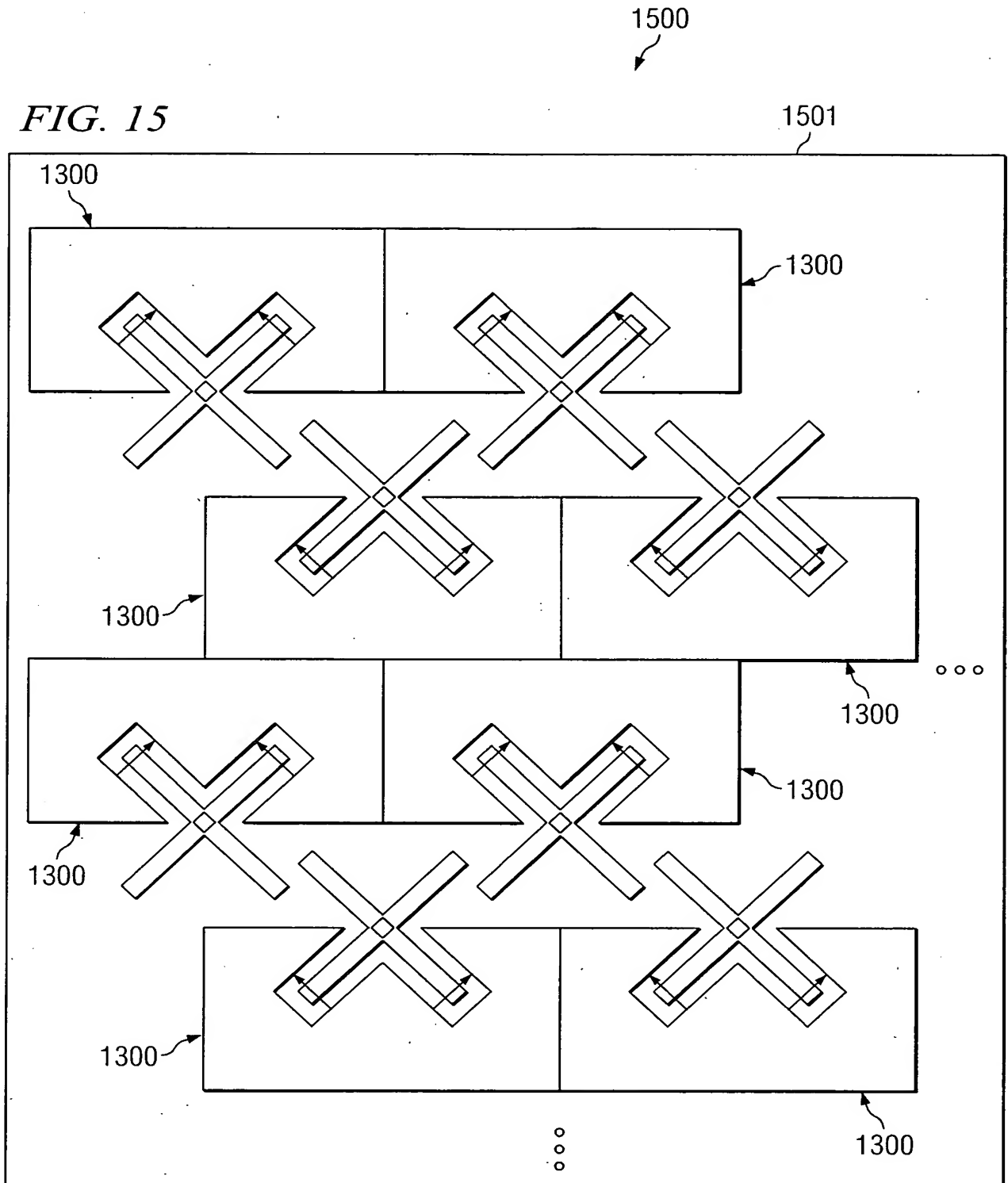
FIG. 9*FIG. 10*

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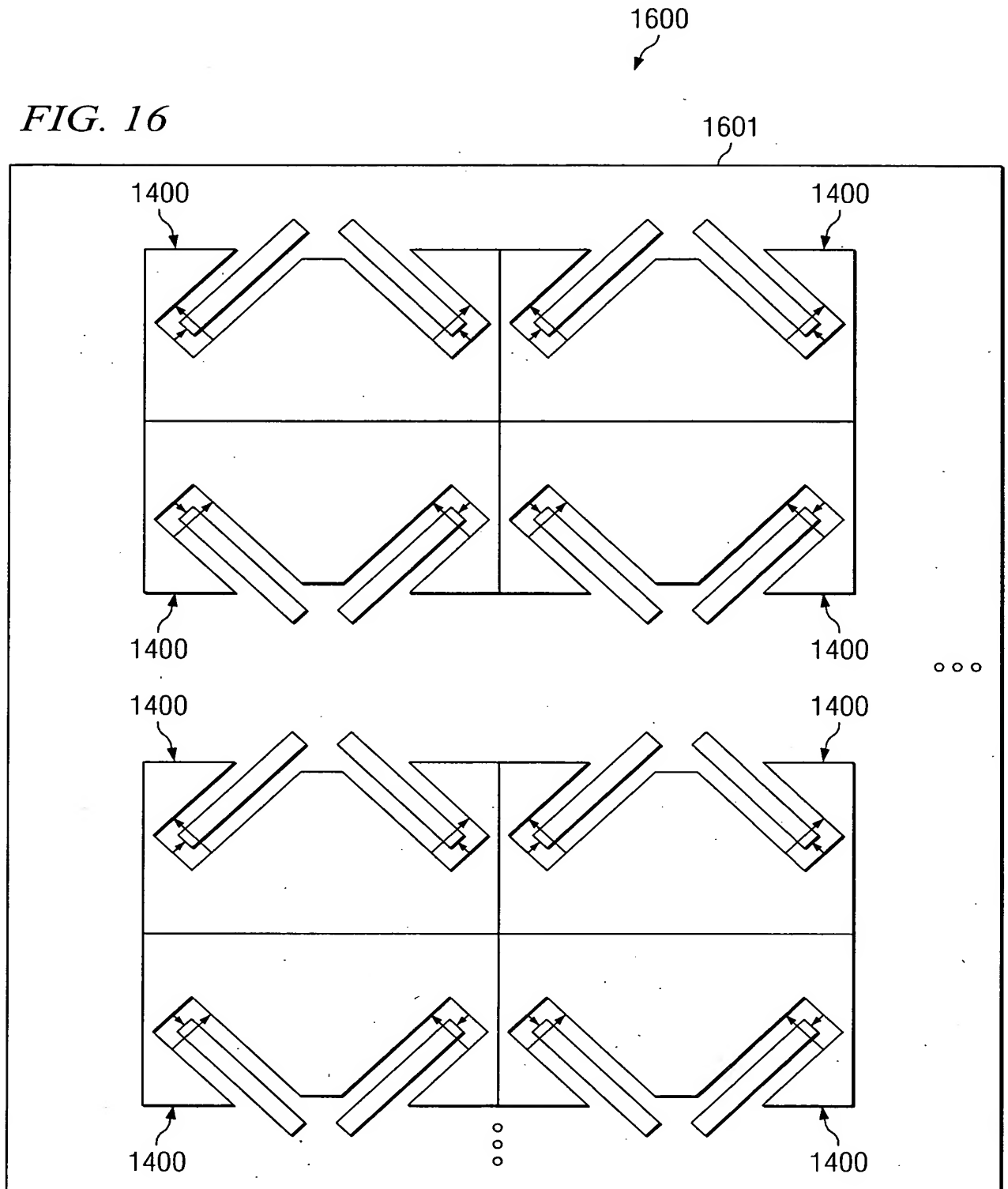
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FIG. 15

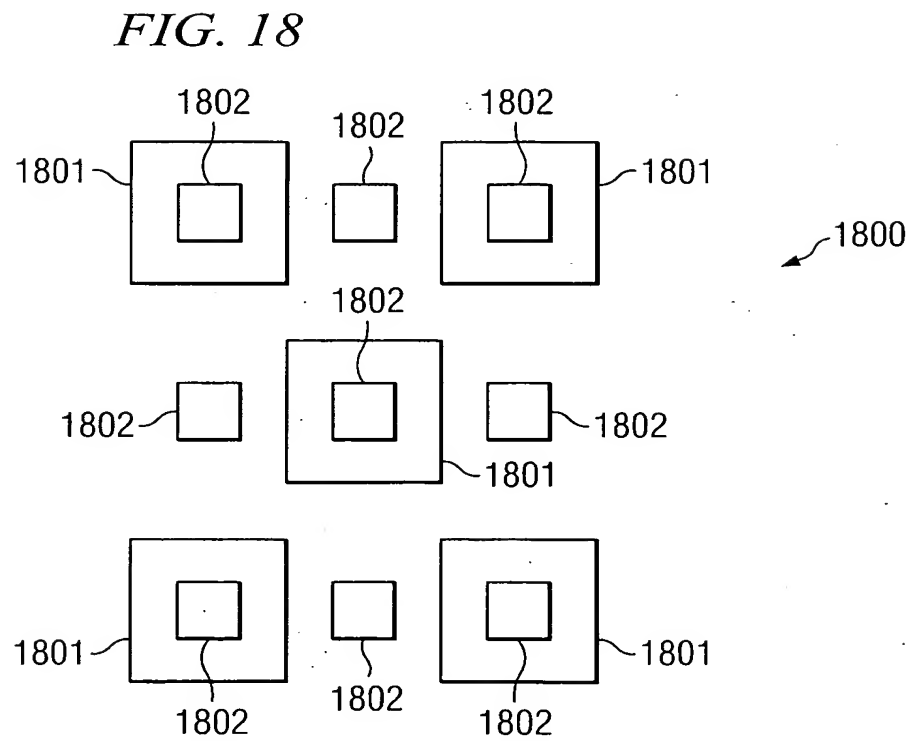
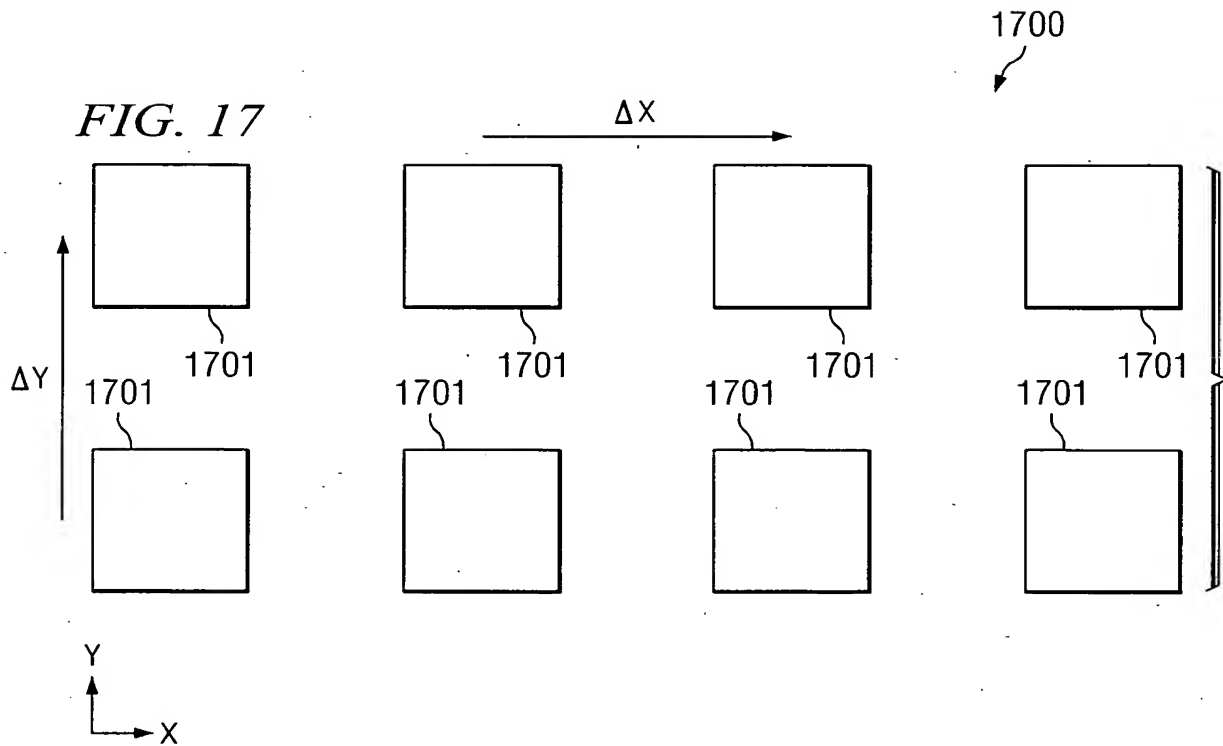


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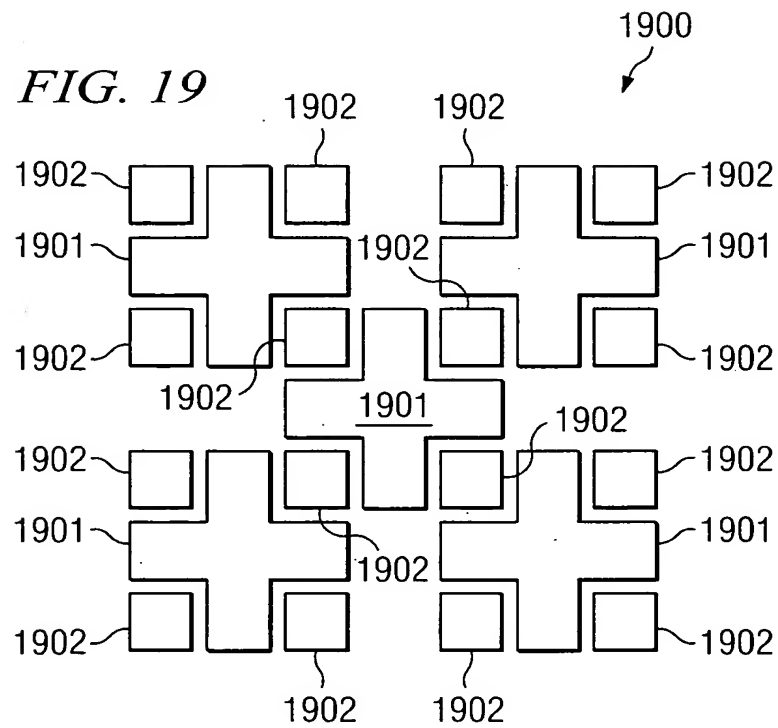
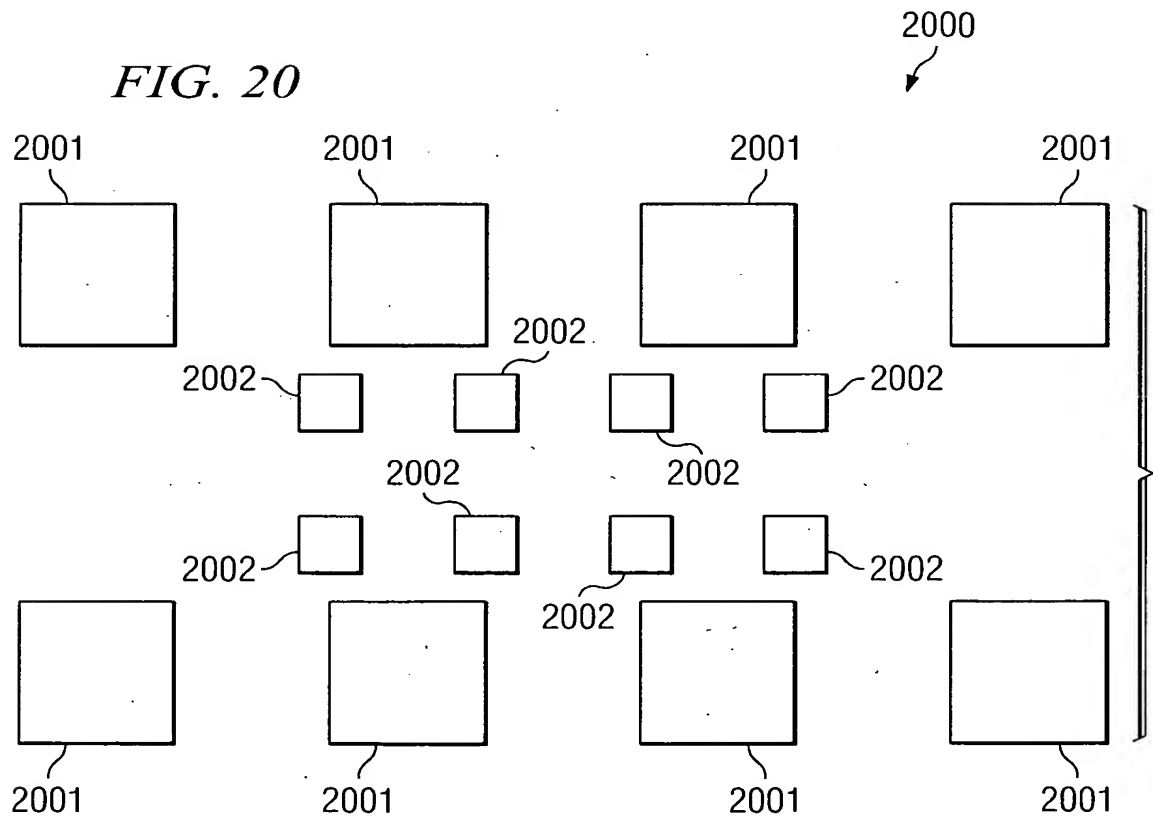
FIG. 16



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FIG. 19*FIG. 20*

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FIG. 21

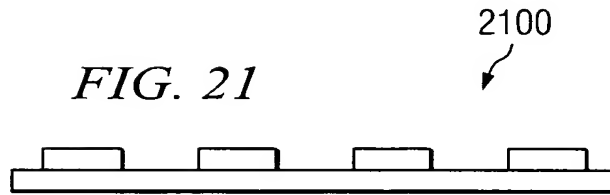


FIG. 22

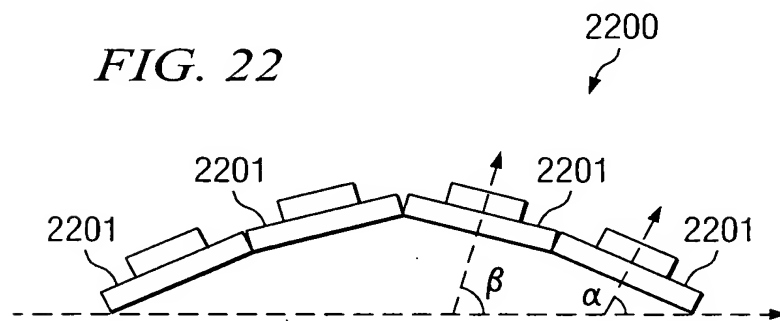
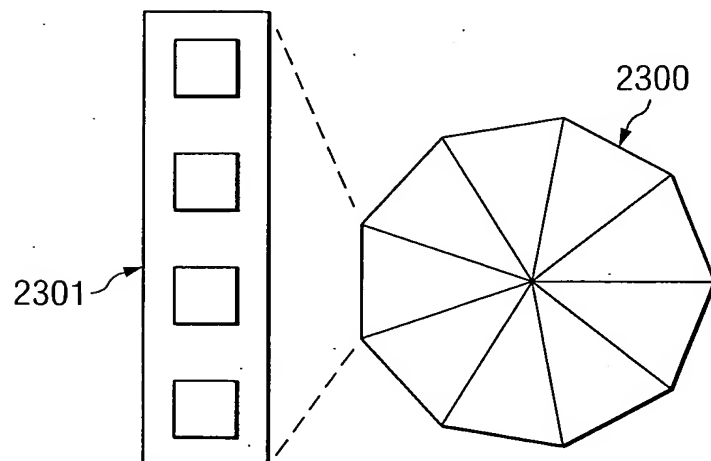


FIG. 23



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FIG. 24

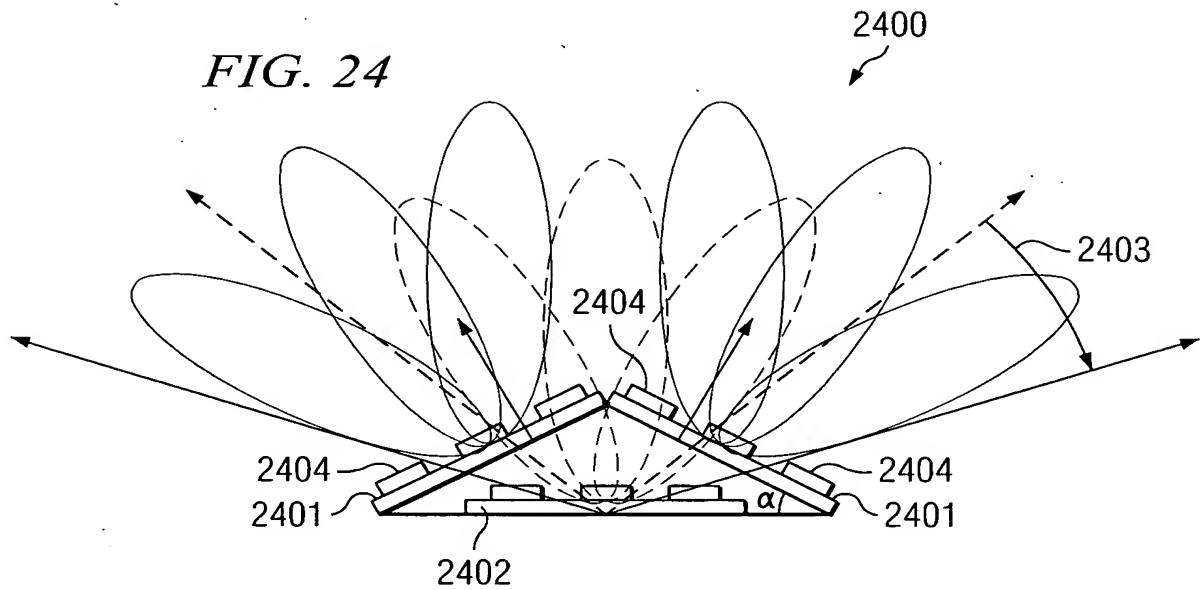
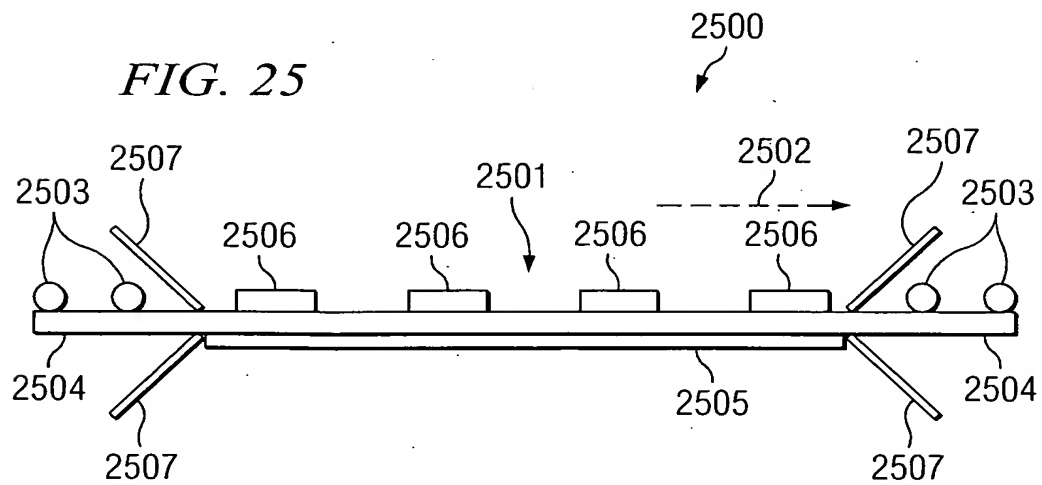


FIG. 25



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FIG. 26

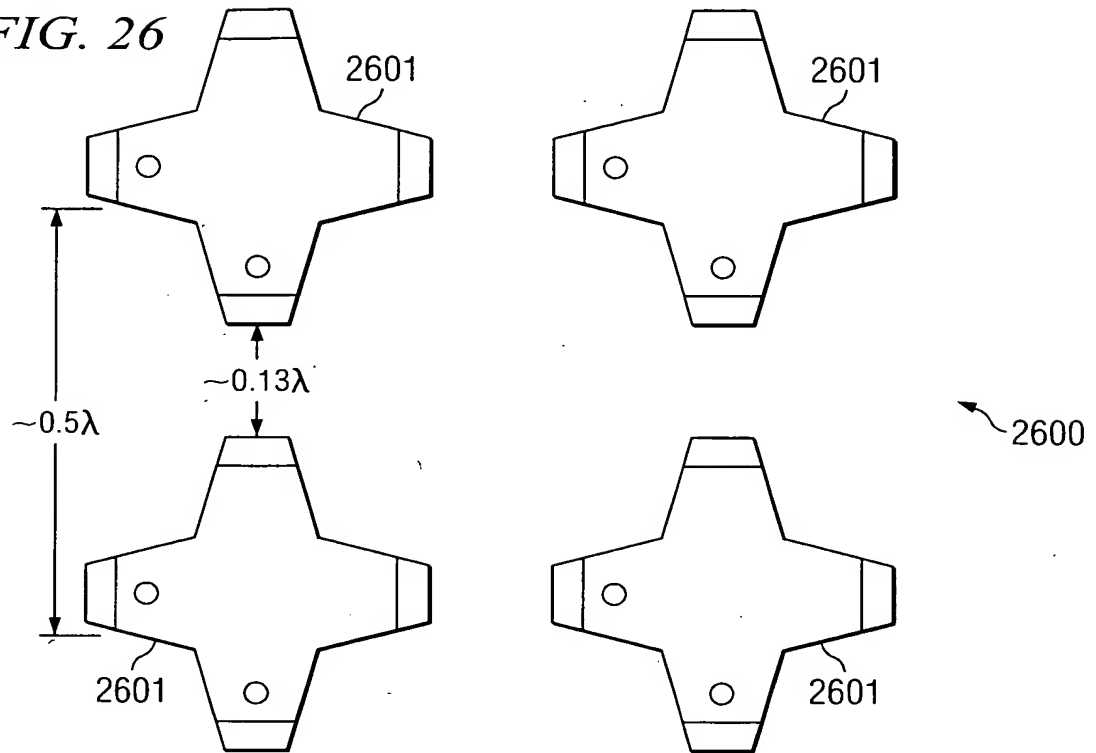
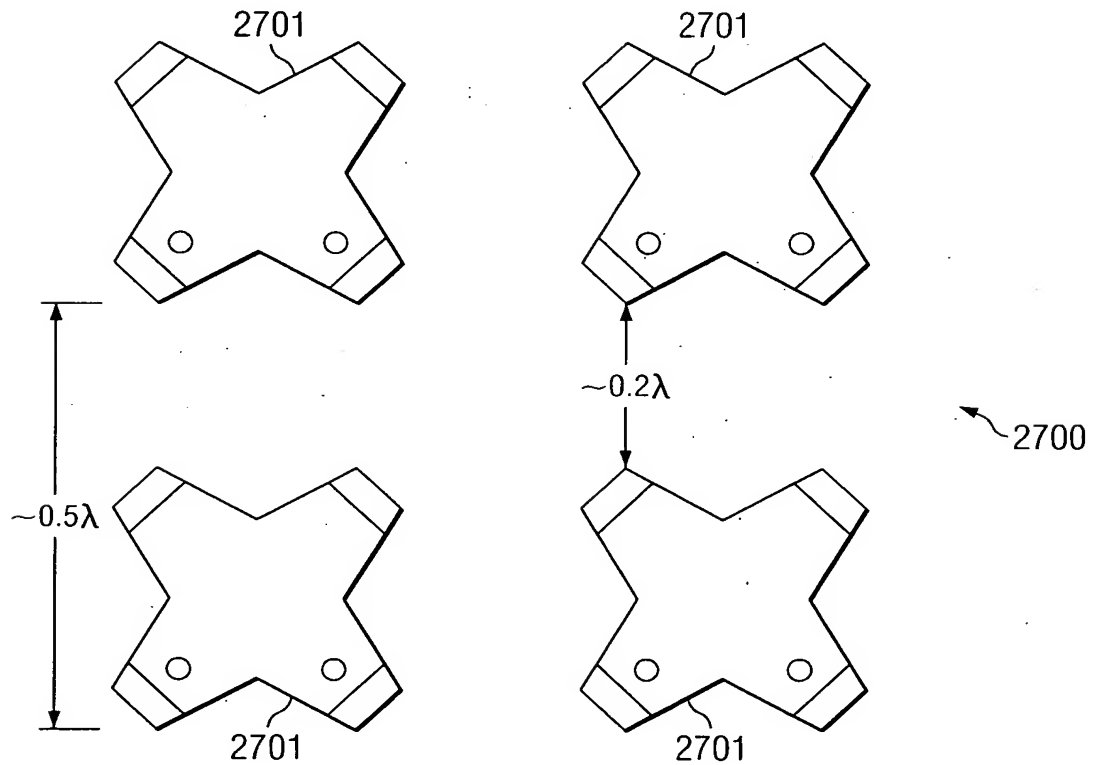


FIG. 27



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FIG. 28

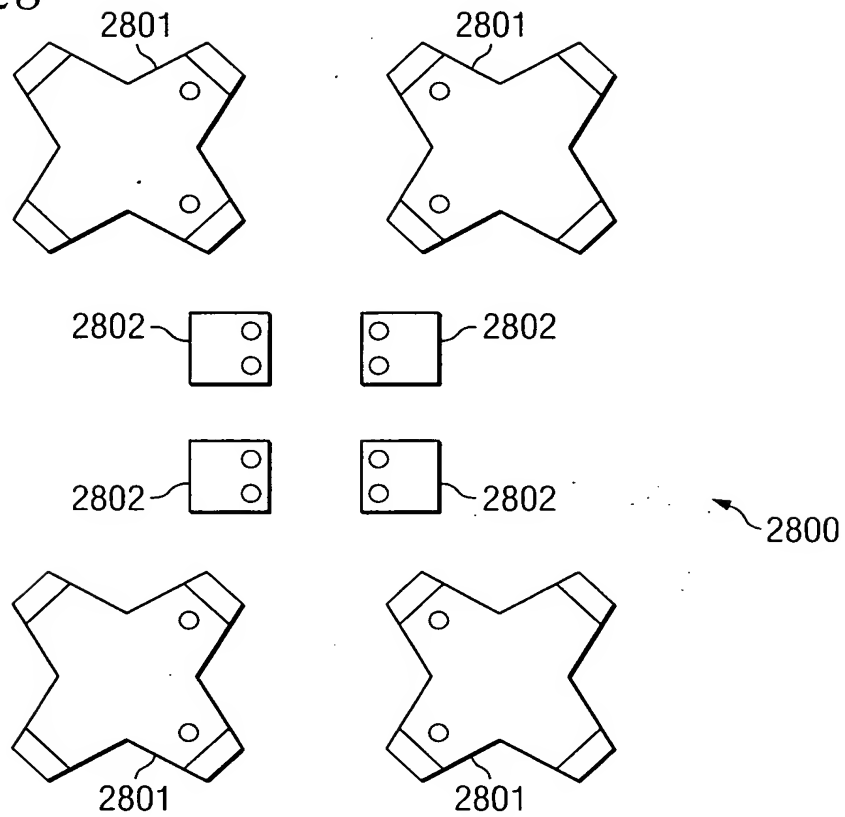
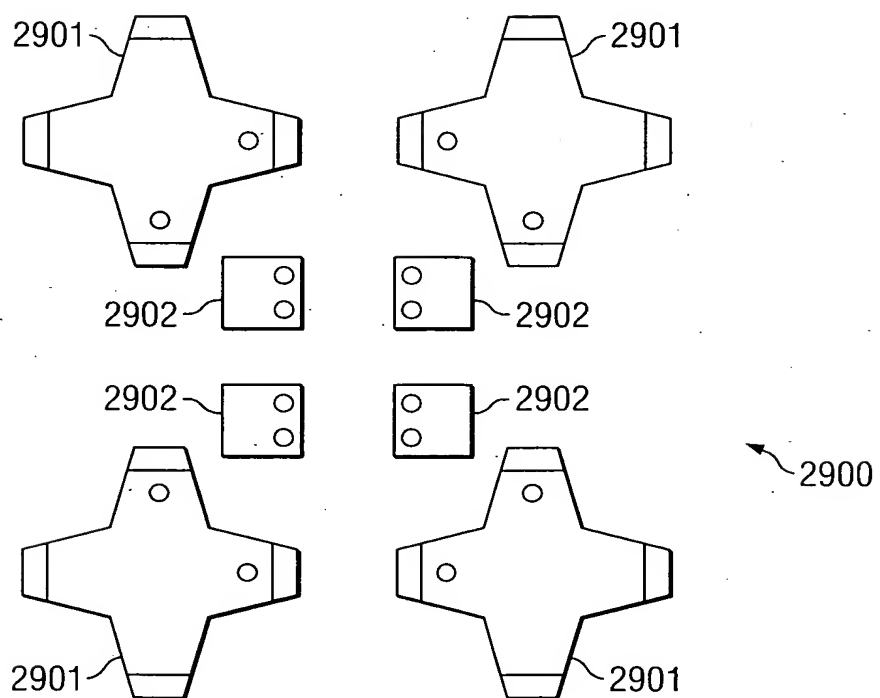


FIG. 29



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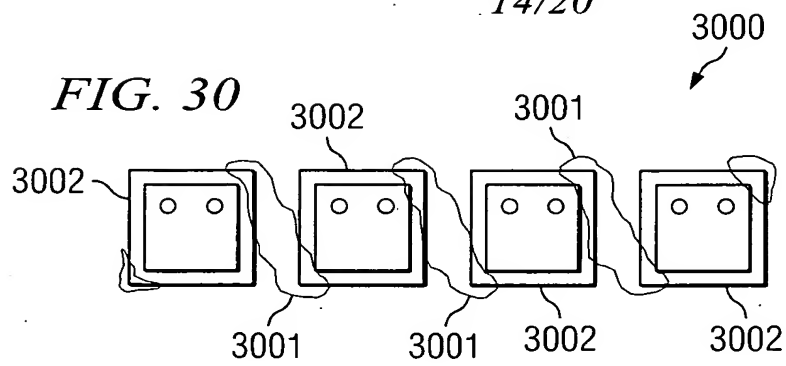
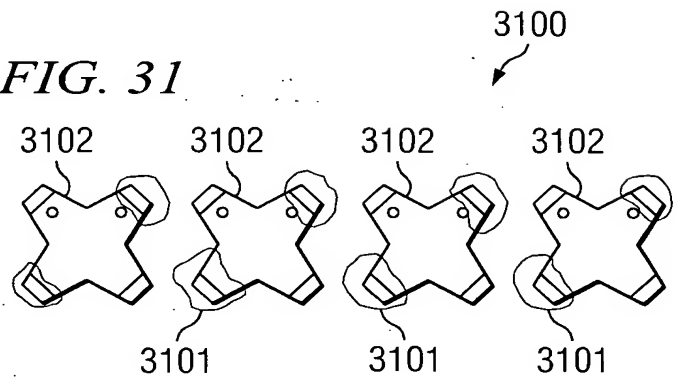
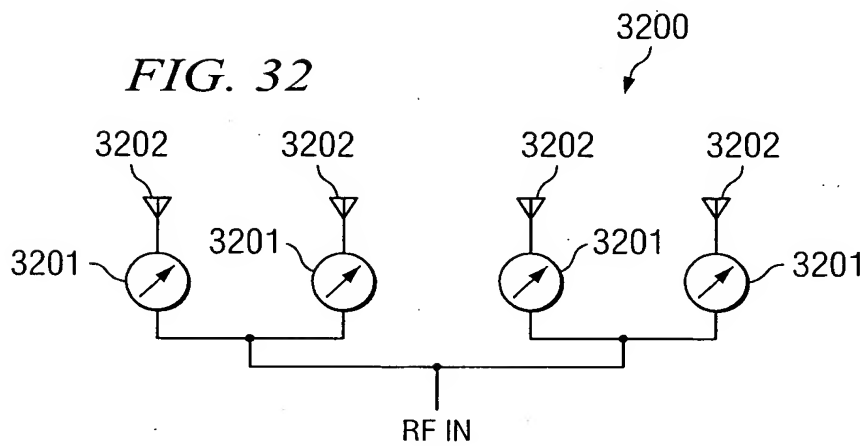
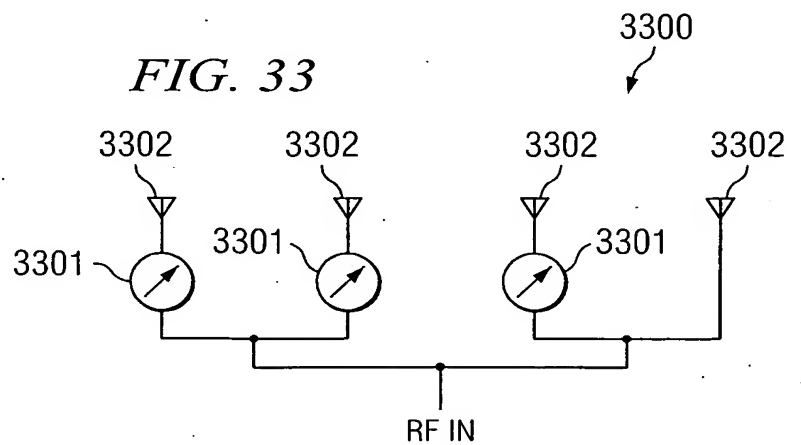
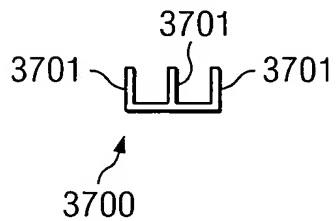
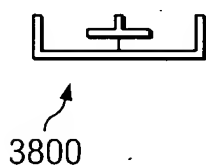
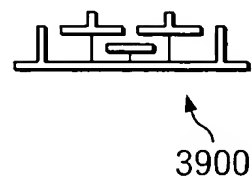
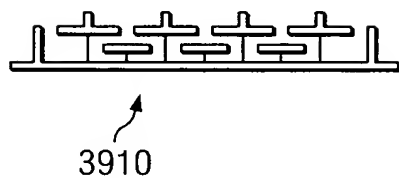
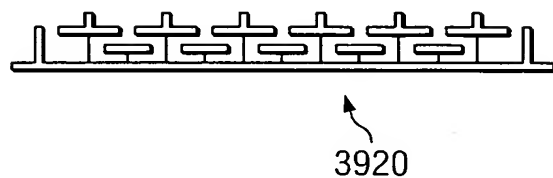
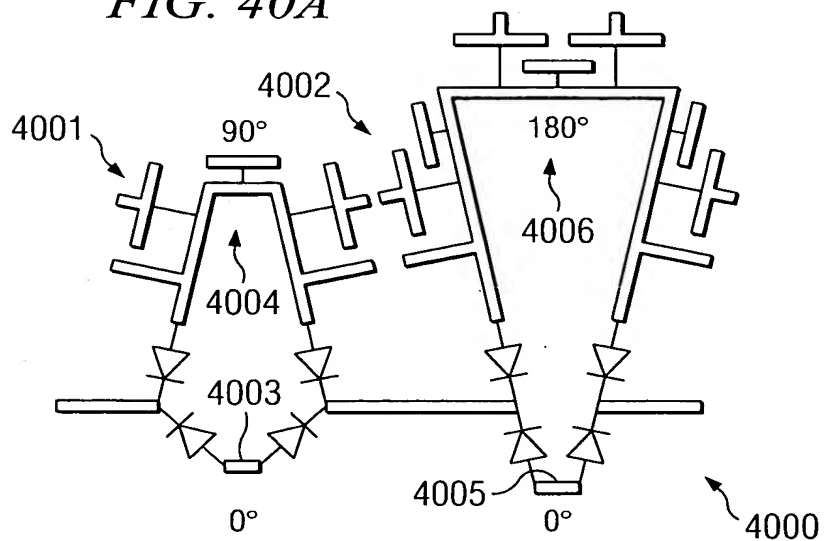
FIG. 30**FIG. 31****FIG. 32****FIG. 33**

FIG. 34

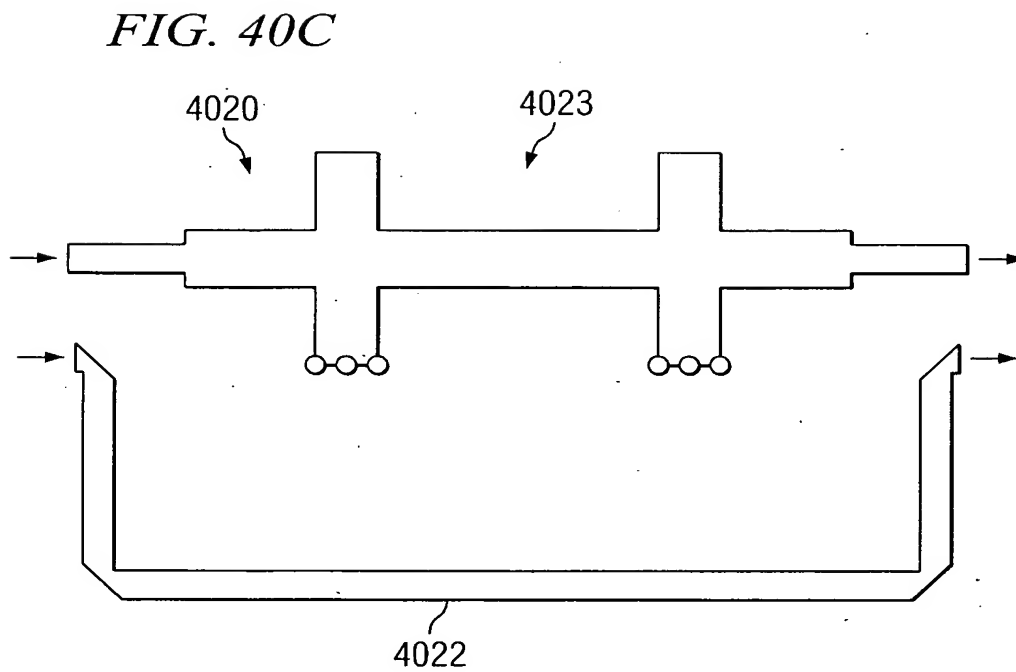
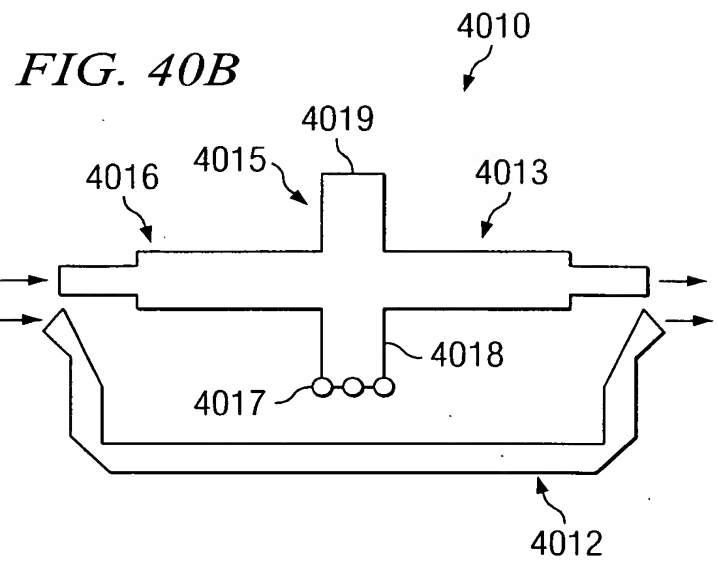
The diagram shows a differential signal processing stage 3400. It consists of two input signal lines, 3403 and 3404, which are connected to a pair of differential transistors, 3401 and 3402. The gates of these transistors are connected to a common biasing network. This network includes a resistor 3405 connected to a supply voltage V_{CC} , and two other resistors connected to ground. The output of the stage is a differential signal, indicated by the voltage difference $\Delta\Phi$ between the gates of the two transistors. The output lines 3403 and 3404 are also connected to ground through resistors.

[illegible]

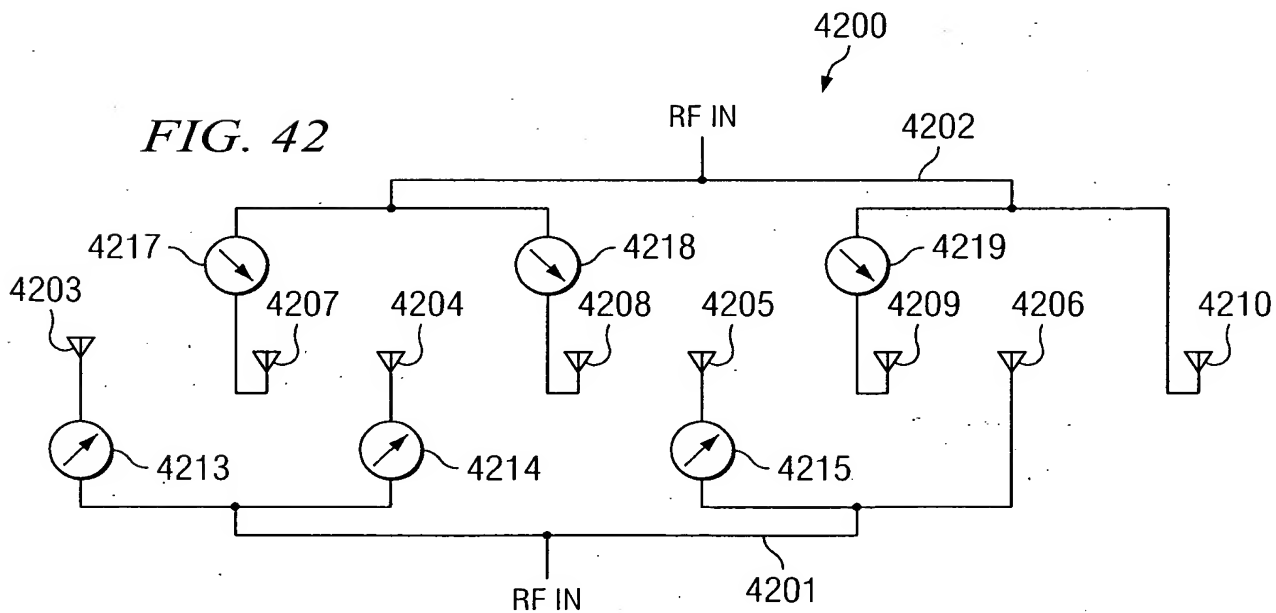
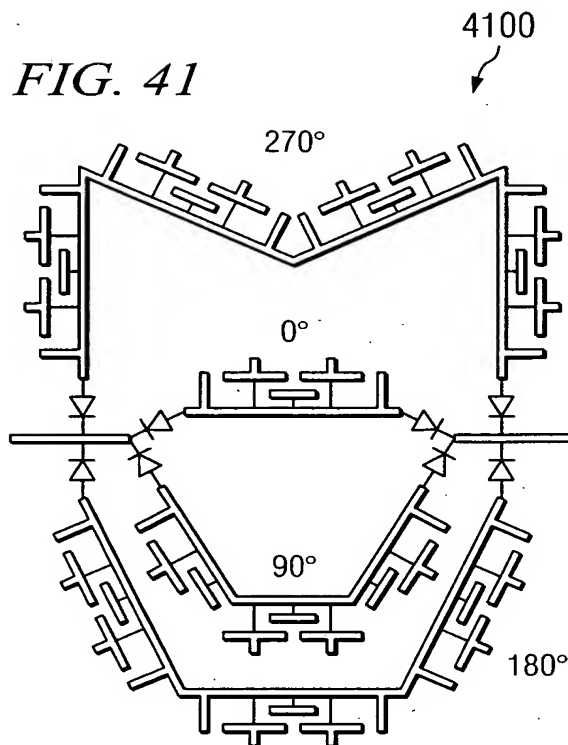
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FIG. 37
(PRIOR ART)*FIG. 38**FIG. 39A**FIG. 39B**FIG. 39C**FIG. 40A*

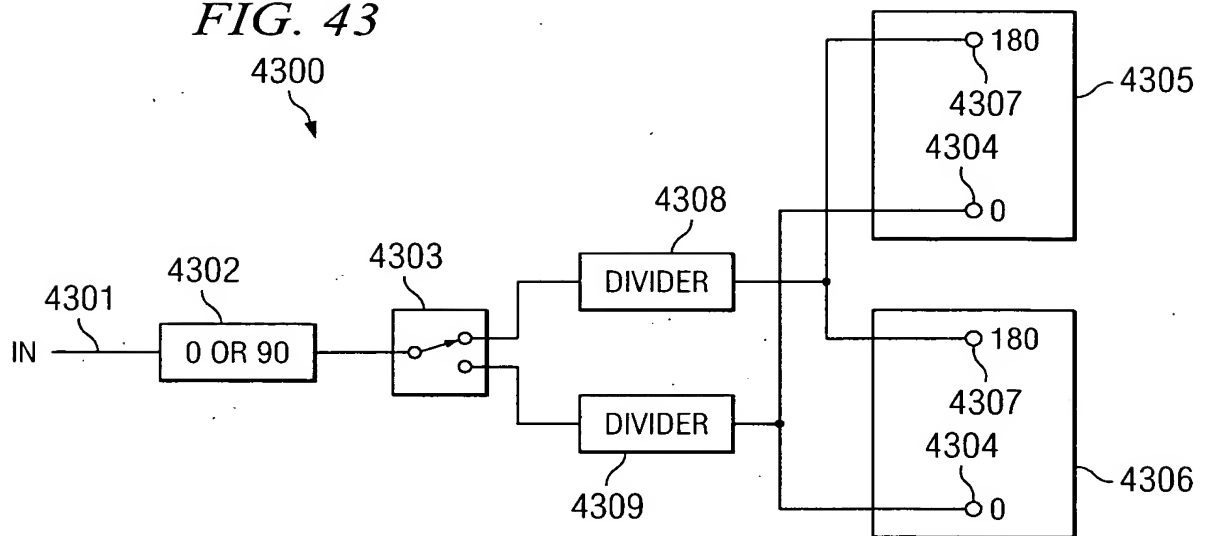
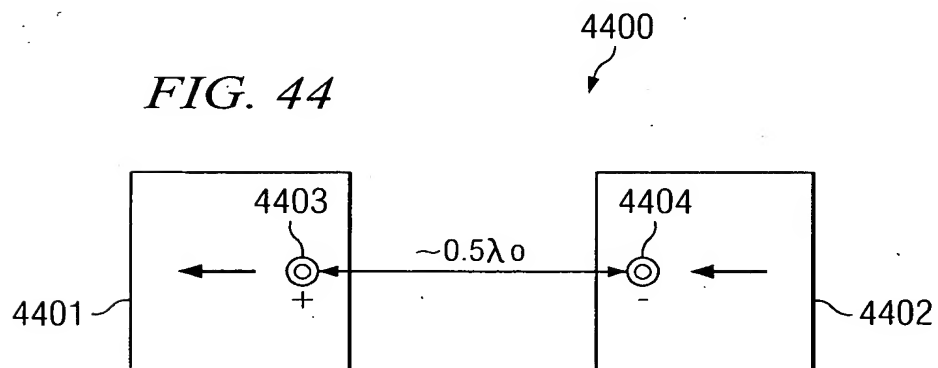
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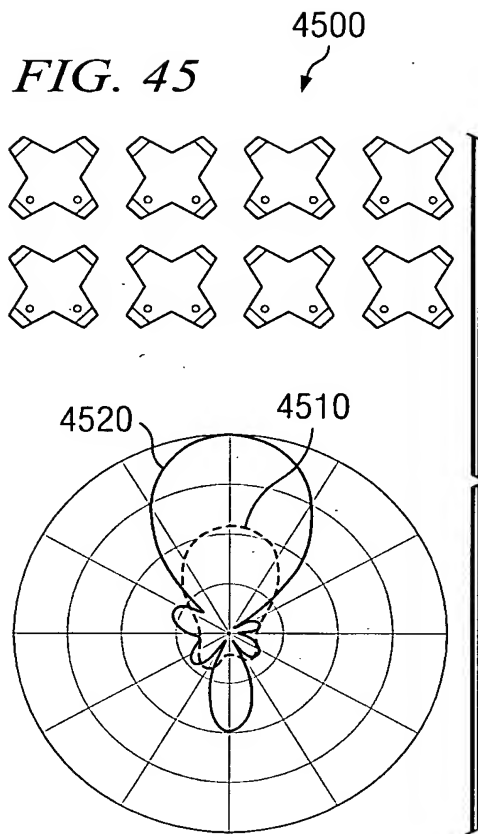
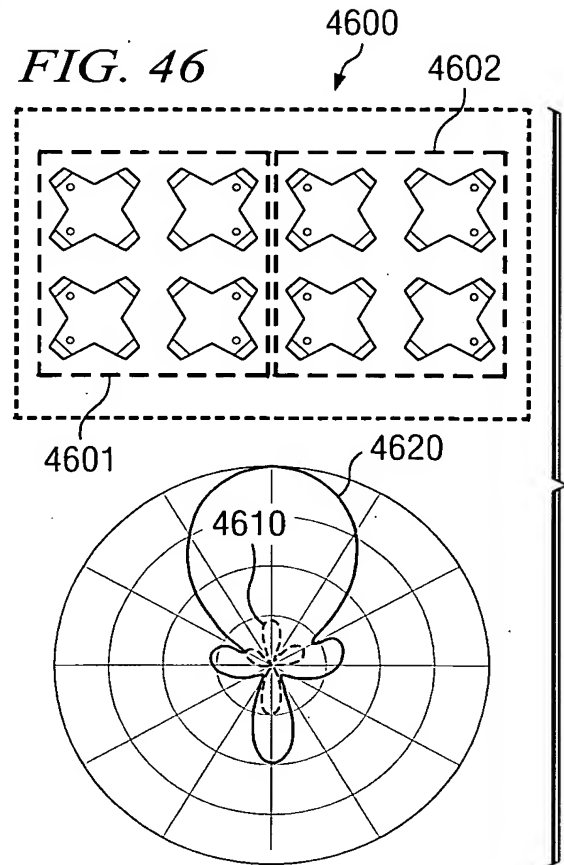
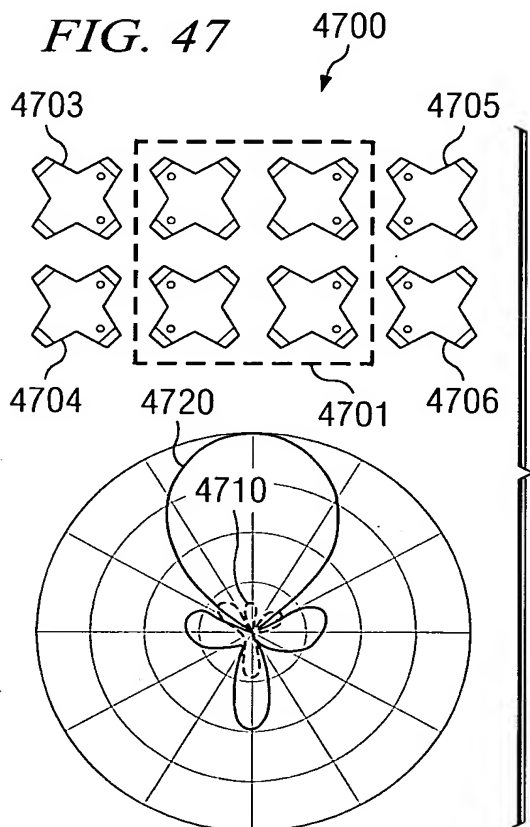
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FIG. 43*FIG. 44*

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FIG. 45*FIG. 46**FIG. 47**FIG. 48*